Digital Adaptive Multimode Synchronous Rectifier Controller HY903

Revision 1.4
Documentation number: DS-HY903-R14

Contents

Digital Adaptive Multi-Mode Synchronous Rectifier Controller

Features

- Low-side synchronous rectification without auxiliary winding
- Supports Multi-Mode operation: DCM, CCM, PFM and QR
- Wide output voltage range: 3-25V
- Wide VCC bias range up to 8V
- High voltage drain sensing up to 120V
- High current gate driver compatible with various MOSFET
- Driver voltage clamped to 8.0V
- Adaptive pre-turn off driver speeding up turn off transition
- Selectable option for T_OFF_MIN
- Self-supply to maintain operation with output voltage as low as 3V
- Shoot through protection (STP)
- Optimized switching loss and EMI
- Low quiescent current

Description

HY903 is a smart digital control synchronous rectifier controller functioning as diode emulator. It drives the standard N-channel Power MOSFET to replace Schottky in order to achieve the high efficiency. HY903 incorporates the digital control technology to optimize the multi-mode operation at DCM/PFM/CCM/QR in the different applications. The digital control technology further enhances the robust CCM operation. Adaptive pre-turning off scheme not only guarantees the fast transition but also minimizes switching loss. The adaptive pre-turn off scheme optimizes the EMI due to the soft SR MOSFET switching off transition. The configurable volt-second threshold through INTG pin avoids SR MOSFET mis-trigger transition due to the parasitic ring under DCM/QR mode. HY903 integrates the multi features to minimize the BOM and optimize the performance.

HY903 is available with SOT23-6 package.

Applications

- USB PD and Quick Chargers
- AC/DC offline adaptor

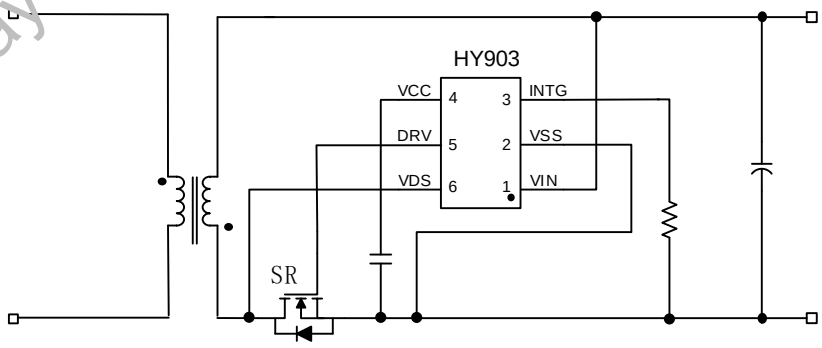


Fig 1. Typical Application Diagram

Option Table

Product		HY903A	HY903B
T_OFF_MIN	1.25 μs	•	
	2.5 μs		•

SOT23-6 (Top view)

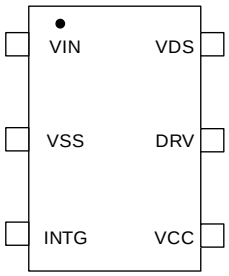


Fig 2. Package Diagram

Pin	Name	Description
1	VIN	HV bias input pin. VIN pin connected to the converter output voltage.
2	VSS	Ground. VSS is used as a MOSFET source sense reference. The PCB trace between VSS and source of SR MOSFET should be designed as short as possible.
3	INTG	Connect INTG pin to VSS pin through a configuration resistor to setup the integral time after SR MOSFET turns off. This prevents the SR controller from turning on falsely by ringing below the turn-on threshold at VDS pin under DCM/QR mode.
4	VCC	IC bias pin. VCC is the supply of the HY903. A typical 1uF to 2.2uF X7R bias capacitor is recommended to be designed in applications
5	DRV	Gate drive output. Connect DRV with the gate of external MOSFET through a resistor in the application. The PCB trace between DRV and gate of SR MOSFET should be designed as short as possible.
6	VDS	MOSFET drain voltage sense. The PCB trace between VDS and drain of SR MOSFET should be designed as short as possible.

Absolute Maximum Ratings (Note 1)

Item	Min	Max	Unit
VCC, DRV	-0.3	9.0	V
VIN	-0.3	28.0	V
VDS	-1.0	120.0	V
INTG	-0.3	6.5	V
T_J (Operation junction temperature)	-25	150	℃
T_S (Storage temperature)	-40	150	℃

Note 1: Stresses beyond Absolute Maximum Ratings may cause permanent damage to the device.

ESD Ratings

Item	Definition	Value	Unit
Electrostatic Discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001	±4000	V
	Charged device model (CDM), per JEDEC specification JESD22-C101	±500	V

Thermal Specification (Note 2)

Item	Value	Unit
RθJA Junction-to-ambient thermal resistance	260	℃/W
RθJC(top) Junction-to-case (top) thermal resistance	135	℃/W

Note 2: The maximum allowable power dissipation is a function of the maximum junction temperature T_J(MAX), the junction-to-ambient thermal resistance $R_{\theta JA}$, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by $P_D(MAX)=(T_J(MAX)- T_A)/R_{\theta JA}$. Exceeding the maximum allowable power dissipation produces an excessive die temperature, causing the regulator to go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.

Electrical Characteristics

VCC = 8V, 25℃ ambient temperature, unless otherwise noted.

Parameter	Description	Test Condition	Min	Typ	Max	Unit
VIN						
VIN_DBL_ST	VIN Voltage Threshold for Doubler Regulation Start	VIN Rising from 0V to VCC Start to Regulate as 4.8V	3.0			V
VCC Bias Supply						
VCC	VCC Clamp Maximum	VIN Rising from 0V to 25V		8.0		V
VCC_ON	VCC POR Threshold	VCC Rising from 0V to 8V	3.8	4.2	4.4	V
VCC_OFF	VCC OFF Threshold IC Shuts Down	VCC Falling from 8V to 0V	2.5	3.0	3.5	V
VCC_ON_HYS	VCC POR Threshold Hysteresis			0.70		V
VCC_REG	VCC Doubler Regulation	VIN Rising from 0V to 25V	4.0	4.8		V
I_CC_NSW	NO Switching Operating Current	VCC= 8V, No Switching	0.4	0.6	0.7	mA
ICC	Operating Current with Switching	VCC= 8V, 65kHz Switching, 4.7nF Cap on DRV		3.6		mA
VDS						
V_DS_ON	DRV ON Threshold	VCC= 8V, VDS falling	-175	-200	-225	mV
V_DS_OFF	DRV Off Threshold	VCC= 8V, VDS rising	-17.5	-20	-22.5	mV
V_DS_REG	DRV Pre-off Threshold		-45	-53	-60	mV
V_ST	Shoot Through Protection Threshold	VCC=8.0		600		mV

Gate Driver						
V_DRV_CLP	Max DRV Clamp Voltage			8.0		V
R_SRC	DRV Pull up Resistor			4.0	8.0	Ω
R_SNK	DRV Pulls Down Resistor			1.0	3.0	Ω
T_ON_DYL	Turn-ON Propagation Delay	DRV load capacitance 4.7nF, VDS falling transition cross V_DS_ON to DRV rising to 10% of logic high		26		ns
T_OFF_DYL	Turn-off Propagation Delay	DRV load capacitance 4.7nF, VDS rising transition cross V_DS_OFF to DRV falling to 90% of logic high		25		ns
T_R	DRV Turn-on Rising Time	DRV load capacitance 4.7nF, 10% to 90% of logic high		18		ns
T_F	DRV Turn-off Falling Time	DRV load capacitance 4.7nF, 90% to 10% of logic high		13		ns
T_ON_MIN	Minimum Turn-on Time		0.7	0.9	1.1	μs
T_OFF_MIN	HY903A Minimum Turn-off Time		1.0	1.25	1.5	μs
	HY903B Minimum Turn-off Time		2.0	2.5	3.0	μs

IC Function Diagram

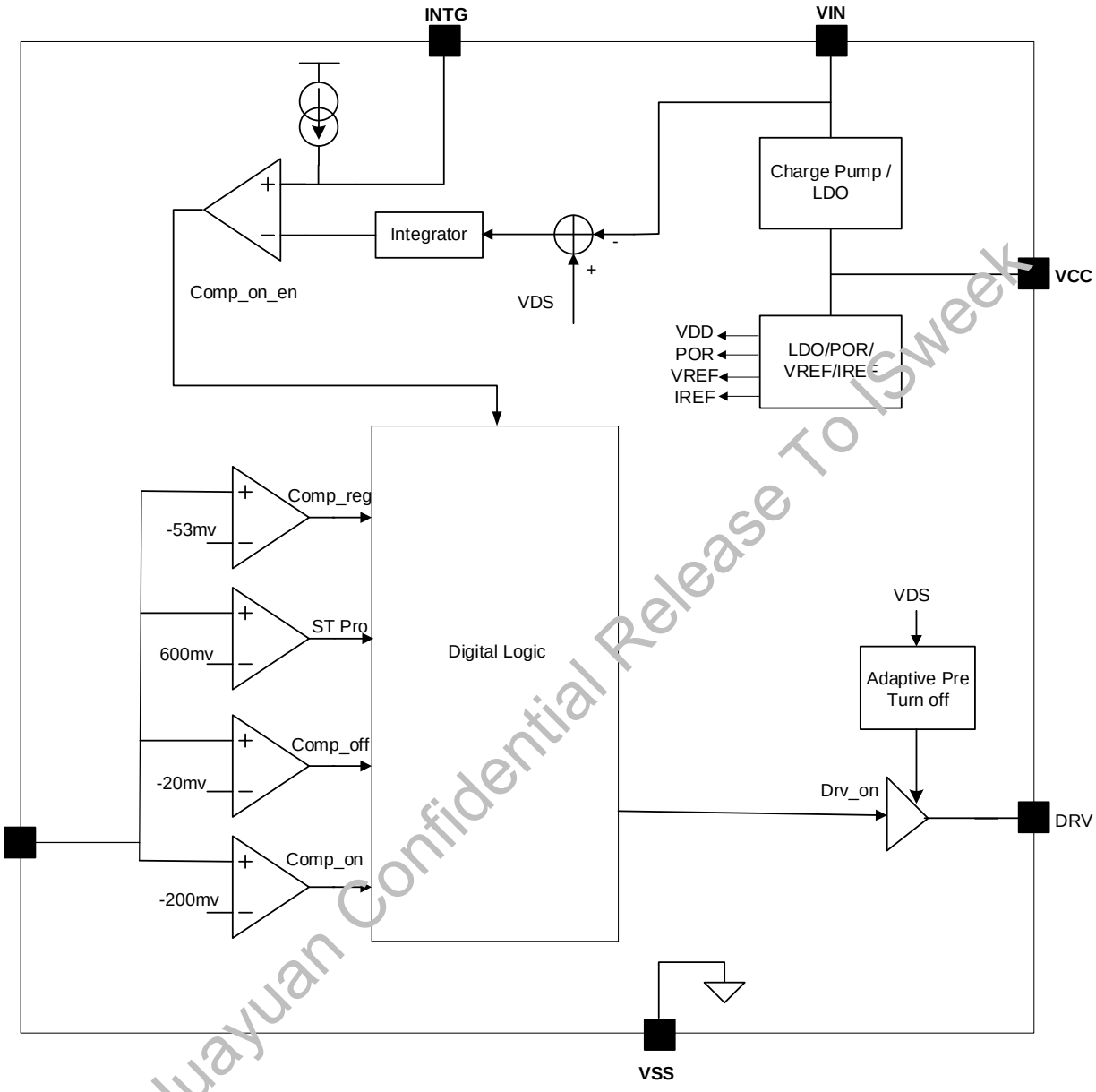


Fig 3. HY903 Function Block Diagram

Detail Function Description

HY903 is a digital control synchronous rectifier controller. It detects VDS of SR MOSFET to control the turning ON/OFF timing. When SR MOSFET VDS is below V_VDS_ON threshold, SR MOSFET is turned on. When SR MOSFET VDS is higher than V_VDS_OFF threshold, SR MOSFET is turned off. The adaptive control scheme of pre-turn off minimizes the turn off transition of the SR MOSFET.

The adaptive pre-turn off scheme improves the EMI due to soft SR MOSFET turning off. It minimizes switching loss due to less conduction overlap between primary MOSFET and SR MOSFET under CCM. A fixed minimum turning on time and turning off time improve the immunity to noise and prevent SR MOSFET mis-triggering due to the current ring noise coupling to VDS signal. VCC internal charge pump and clamp circuit make HY903 operate reliably under wide range of Vin. Vin connects with DC output directly.

VCC Bias

The VCC bias diagram is shown in Fig 4. HY903 is powered from VIN and generates the power supply for the internal circuits at VCC. HY903 incorporates the charge pump circuit to regulate the VCC voltage at 4.8V at the VIN ranges of 3.0V to 5V, and incorporate the voltage follower at the VIN range of 5V to 8V, and then VCC is clamped at 8V if the VIN is above 8V. When VCC reaches VCC_ON threshold, HY903 consumes normal operating current. When VCC is decreased as low as VCC_OFF, HY903 shuts down.

A typical 1uF to 2.2uF X7R capacitor is recommend between VCC and VSS with short trace.

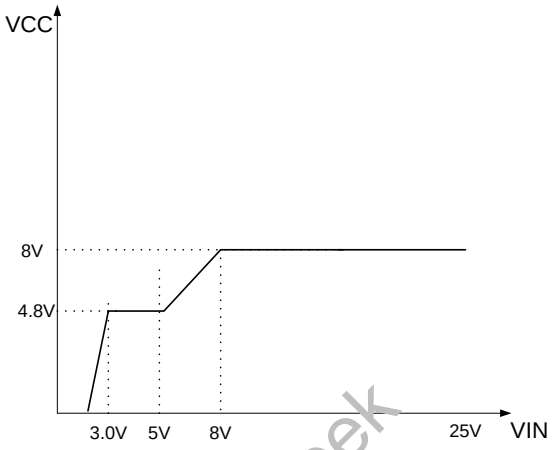


Fig 4. VIN and VCC Bias Diagram

SR MOSFET Control Scheme

SR MOSFET Turning On

The voltage drop across the drain and source of SR MOSFET is sensed from VDS pin and VSS. When primary MOSFET turns off, the VDS voltage of SR MOSFET sharply drops from positive to negative. This transition duration is tens of nanoseconds depending on different applications. The threshold to determine the SR MOSFET turning on is V_DS_ON. When VDS signal is below V_DS_ON during falling transition, HY903 turns on SR MOSFET with minimum turning on delay. To minimize turning on transition time and turning on delay is one of the important factors to reduce the switching loss of flyback converter. After SR MOSFET turns on, a minimum turning on time window is designed in HY903 to mask the mis-trigger turning off scenario due to the current ring right after the SR MOSFET turns on.

SR MOSFET Turning Off

VDS pin continuously senses the drain-source voltage after SR MOSFET turns on. The voltage signal applies to VDS pin is negative Rds_on voltage drop during the SR MOSFET conduction. To minimize the conduction loss of SR MOSFET, the

voltage drops across the VDS should be minimized. HY903 regulates SR MOSFET gate voltage when VDS sign across the threshold V_DS_REG. Once VDS voltage across V_DS_REG, DRV pin continuously drops gate signal voltage and maintain VDS voltage as V_DS_REG , as shown in Fig 5. This scheme prevents SR MOSFET from premature turning off. In the meantime, the turn-off transition and delay time of SR MOSFET is minimized from this pre-turn off scheme.

When the secondary current drops and the VDS voltage signal across the V_DS_OFF threshold, the SR MOSFET turns off. After SR MOSFET turns off, a minimum turning off time window is designed in HY903 to mask the mis-trigger turning on scenario due to the current ring right after the SR MOSFET turns off, as shown in Fig 5. When the system operates under CCM, the waveform is shown as in Fig 6. It is noticed that, the pre-turning off time can be very short or totally disappeared under CCM operation.

It is noted that, a fixed turning off blanking timer does not always work well for the entire range of line and load conditions in different applications. A flyback under quasi-resonant (QR) operation, system may operate in DCM under light load condition. In this case, the turning off blanking time should be long enough to avoid DCM ringing causing SR false turning on. On other hand, when the converter operates in QR mode under high input voltage, the primary side MOSFET switching on-time is short, and the minimum off-time may cut into the conduction of the SR. In this case, there is an extra conduction loss as the body diode of SR MOSFET conducts if the minimum off-time masks the beginning portion of SR MOSFET turning on. There are two options on the minimum turning off time corresponding to HY903A and HY903B for the different applications. They are listed in product option table.

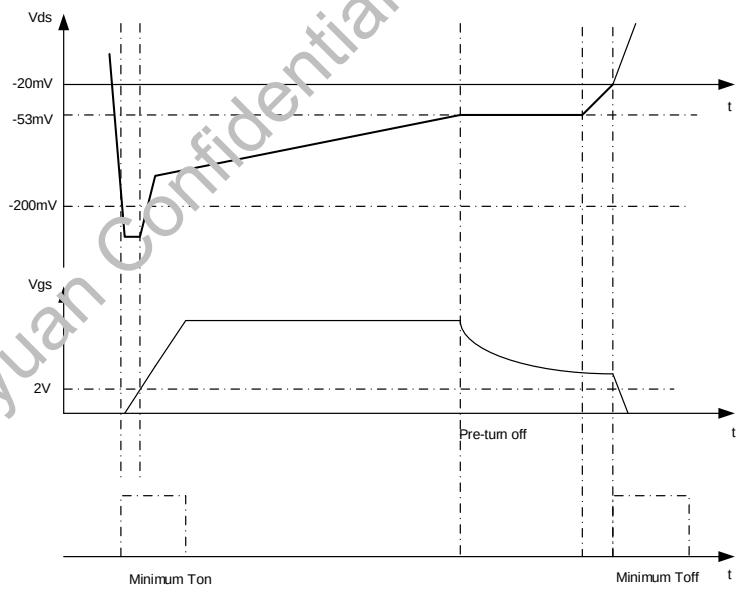


Fig 5. SR MOSFET Turning ON/OFF Diagram under DCM

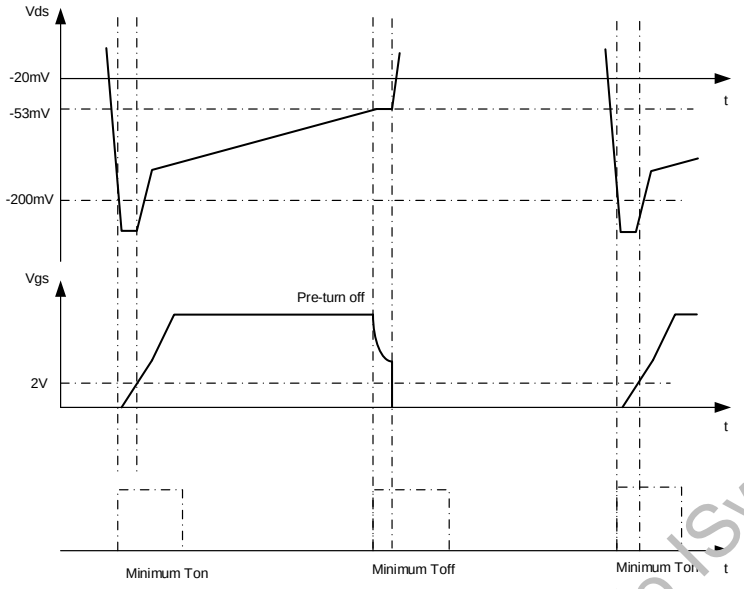


Fig 6. SR MOSFET Turning ON/OFF Diagram under CCM

INTG Pin Configuration

In DCM or QR mode, there is substantial ring that is resonant by magnetic inductance and the parasitic capacitance after secondary current resets. This ring can possibly trigger the V_DS_ON threshold and turn on SR MOSFET again after it turns off. This causes multiple pulses on SR MOSFET in one switching period. This also causes extra loss, EMI and potential reliability issues. The minimum off time window is designed to mask this mis-trigger scenario. In addition to the minimum turn off window of SR MOSFET, HY903 is designed with configurable pin, INTG, to achieve reliable SR MOSFET switching transition.

INTG pin is used to configure the volt-second product of V_{DS} above output voltage applied to VIN pin as shown in Fig 7. An external resistor R_{ext} is designed and connected on INTG pin to VSS in the application system. The configurable volt-second product threshold is determined by INTG*R_{ext}. This is shown by the area I in Fig 7. The INTG is a designed coefficient inside of IC. The volt-second product of V_{DS} above output voltage applied to VIN pin is shown in the area II in Fig 7. In normal operating, only when area II is equal or larger than area I, the SR MOSFET turns on once VDS pin is below V_DS_ON threshold during falling edge.

In HY903, if the VDS volt-second product above VIN is below the INTG pin configured threshold defined by area I, SR MOSFTE does not turn on. This scheme guarantees that the SR MOSFET can not be mis-triggered on by the parasitic ring before primary MOSFET turning on. The volt-second product is reset in every switching cycle. Therefore, there is no multiple pulses happening due to the parasitic ring that can potentially triggers the SR MOSFTE turning on condition. This scheme also avoids the potential mis-trigger turning on of SR MOSFET by noise coupling VDS pin.

In HY903 application, a typical value of 10kΩ is used to connect on INTG pin to VSS.

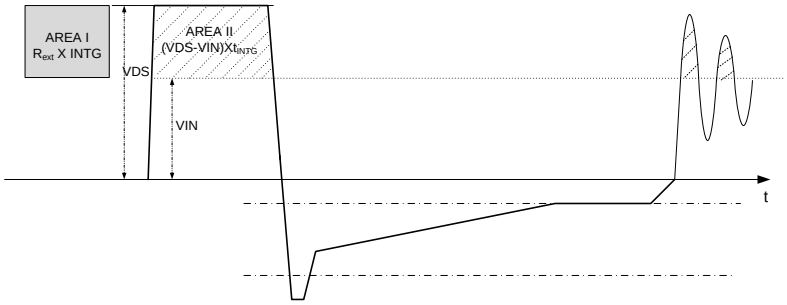


Fig 7. INTG Pin Configuration Diagram

DRV Pull Down and Drive

During the power on, an internal switch control block pulls down DRV pin before in internal circuit POR. This internal pulls down circuit secures no SR gate drive signal before VCC rising above VCC_ON.

HY903 clamps the gate driver voltage to a maximum level of 8.0V in order to achieve the fast switching transition and low switching loss. Based on high voltage MOSFET characteristics controlled by HY903, 8.0V clamp internally gate driver is designed to minimize conduction loss in the applications.

It is noted that, the IC internal comparator propagation delay, comparator output rising time, gate driver delay and SR MOSFET turning on delay together constitutes total delay before SR MOSFET turning on. During this delay time, the SR MOSFET body diode is conducting. The more time of the SR MOSFET turning on delay, the more time for body diode conducting, and the more body diode forward loss. The gate driver source and sink resistance are designed to achieve fast turning on and turning off transition as shown in the electrical characteristics table. In applications, it is required to minimize the delay by optimizing gate resistor and PCB trace between DRV and SR MOSFET gate in order to achieve the fastest SR MOSFET transition time.

Shoot Through Protection (STP)

In any cases, if primary switch turns on while SR MOSFET is still on, the current on the secondary side conducts from drain to source of SR MOSFET. This current direction is reversed from the normal secondary current that charges output cap. This current discharges output DC cap and rises sharply as it is a shoot through current.

HY903 designs an internal shoot through protection (STP) by a fast comparator. The threshold of the STP is 600mV. Once the voltage on VDS pin triggers the shoot through protection threshold, V_ST, the SR controller shuts down the SR MOSFET immediately. This STP function effectively protects primary MOSFET and SR MOSFET from blowing up.

Application

HY903 SR controller is designed for high performance AC to DC offline solution. It is designed to control the secondary side MOSFET to perform as diode emulator circuit. HY903 can achieve high efficiency, low EMI, low BOM and high reliability application system. The typical AC/DC offline application diagrams that HY903 is connected at low side on the secondary are shown in Fig 8. In these application diagrams, the primary controller is HY1601. It is recommended that a 470 Ω resistor is connected between source of SR MOSFET and VDS pin of HY903.

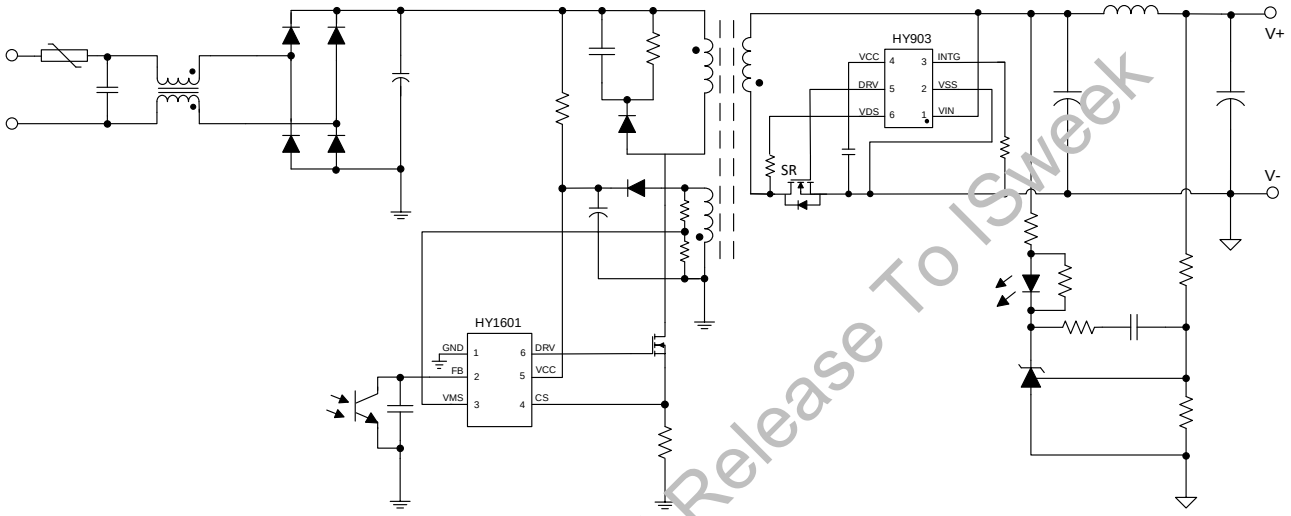


Fig 8. Application Diagram of HY903

SR MOSFET Selection

As an application example, an AC/DC flyback adaptor design specification is listed as: Po=45W, Vo=15V, Io=3A, Efficiency η=88%, min. AC input V_{inrms_min} = 85V, max. AC input V_{inrms_max} = 265V, transformer turn ratio N = 7. It is assumed that the minimum DC bus voltage is 65% of the peak voltage of DC bus in this case. Under QR mode, minimum DC bus voltage and full load condition, the secondary peak current is calculated as below steps:

$$V_{dcbus\_min} = \sqrt{2} * V_{inrms} * 65\% = 78.14\,V \quad (1)$$

Under QR mode, duty cycle is calculated as

$$d = \frac{N*V_o}{V_{dcbus\_min}+N*V_o} = 57.3\% \quad (2)$$

Primary peak current is calculated as:

$$I_{p\_pk} = \frac{P_{in}/V_{dcbus\_min}}{d} * 2 = 2.28A \quad (3)$$

Secondary peak current is calculated as:

$$I_{s\_pk} = I_{p\_pk} * N = 15.98A \quad (4)$$

The maximum forward voltage drop across SR MOSFET is suggested less than 100mV under the peak current condition in order to minimize conduction loss on SR MOSFET. The R_{ds_on} of SR MOSFET is calculated as:

$$R_{ds\_on} = \frac{0.1}{I_{s\_pk}} = 6.26\,m\Omega \quad (5)$$

Under high temperature, R_{ds_on} increases as the temperature rises. The typical R_{ds_on} is increased to be 150% to 180% from 25°C to 125°C junction

temperature. In this application example, R_{ds_max} as 10 mΩ under full load operation and 125°C operating junction temperature can be used for the calculation. The secondary side pre-off current of SR MOSFET is calculated as:

$$I_{s\_preoff} = \frac{V\_DS\_REG}{R_{ds\_max}} = 5.3\ A \quad (6)$$

Where V_DS_REG is selected as -53mV. VDS rating of SR MOSFET is calculated based on 90% derating and 120% scale factor considering spiking voltage when SR MOSFET turns off as:

$$V_{DS} = (\frac{V_{in_{max}} * \sqrt{2}}{N} * 120\% + V_o)/90\% = 88.05V \quad (7)$$

A 100V MOSFET is selected in this example.

VCC Bypass Cap

For stable internal regulator bias on IC circuit, enough external VCC bypass capacitance is designed in the application system. A typical 1uF to 2.2uF X7R capacitor is recommended to function as bias cap on VCC pin, as shown in Fig 9. The 1uF to 2.2uF X7R capacitor selection is after considering the capacitance drop due to DC voltage bias on the capacitor in the applications. The VCC bias cap is located as close as possible to VCC and VSS ground to bypassing noise and ripple on the layout in PCB design.

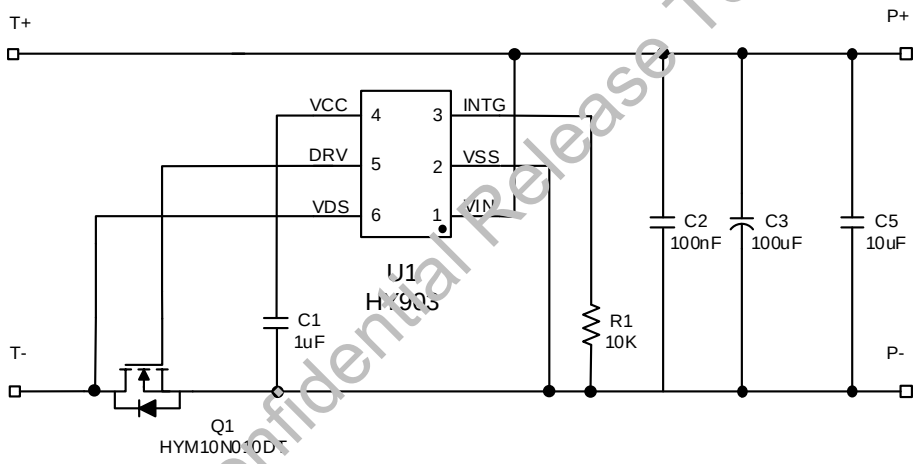


Fig 9. HY903 EVB Schematics

HY903 Evaluation Board

HY903 EVB is designed for customers to do the evaluation on HY903. The schematics is designed and shown in Fig 9. The BOM is listed in Table 1.

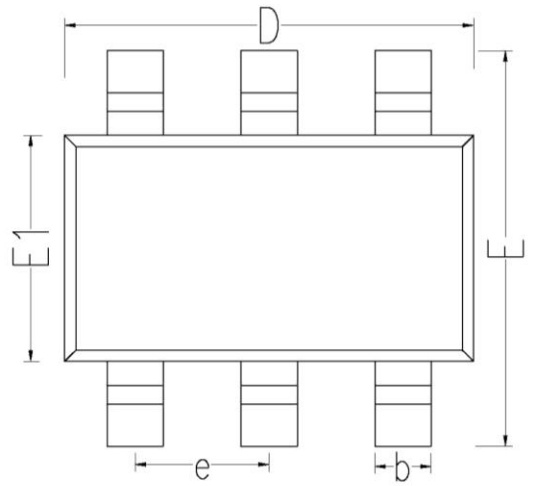
Layout

1) VCC bypass cap: the low ESR ceramic capacitor is required to be as close as possible to VCC and VSS pins on PCB layout.
2) VDS pin to the drain of SR MOSFET and VSS pin to the source of SR MOSFET layout trace should be as short as possible.
3) DRV pin to the gate of SR MOSFET trace, including the gate resistor, should be as short as possible. The loop from DRV to the gate of MOSFET, and the source of MOSFET to VSS should be minimized on layout.
4) A100nF ceramic cap is recommended to connect VIN pin as close as possible if necessary.

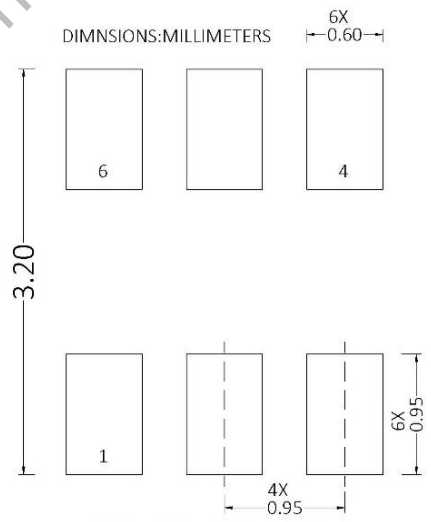
Table 1: EVB BOM List

Components	Specification	Designator	Qty
HY903	HY903, SOT23-6	U1	1
SMD Resistor	10kΩ±5% 1/4W 0603 RoHS	R1	1
SMD Ceramic Capacitor	100nF±10% 50V X7R 0603 RoHS	C2	1
Capacitor	100uF±20% 25V 6.3X6.3mm RoHS (Optional)	C3	1
SMD Ceramic Capacitor	1uF±10% 50V X7R 0603 RoHS	C1	1
SMD MLCC Capacitor	10uF±20% 25V X5R 0805 RoHS	C5	1
N-CH MOSFET	HYM10N010DT 10mohm 100V PDFN 5x6-8L	Q1	1

Package SOT23-6

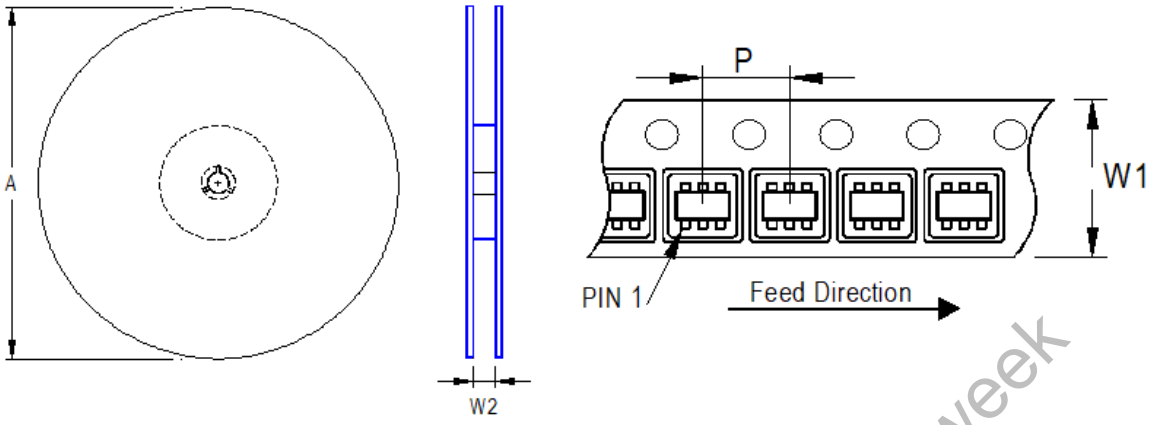


COMMON DIMENSIOS(millimeter)			
SYMBOL	MIN	NOM	MAX
A	-	-	1.45
A1	0	-	0.15
A2	0.90	-	1.30
b	0.30	-	0.50
c	0.08	0.13	0.20
D	2.65	2.90	3.15
E	2.60	2.80	3.00
E1	1.40	1.60	1.80
e	0.95REF		
e1	1.90REF		
L	0.50	0.60	0.70
L1	0.30	0.45	0.60



Recommended Land Pattern

Tape and Reel Information



Package Type	Tape Size (W1) (mm)	Pocket Pitch (P) (mm)	Reel Size (A)		Q'ty Per Reel pcs	Reel Width (W2) Min./Max. (mm)
			mm	inch		
SOT23-6	8	4	180	7	3000	8.4/9.9

PACKING INFORMATION

Item	Package	Pcs/reel	Reel/Reel box	Reel Box Size (mm)	Reel box/Carton Box	Carton Box Size(mm)	Pcs/carton Box
1	SOT23-6	3000	10	210*210*210	4	445*445*230	120000

Notice

HYASIC reserves the right to make corrections, enhancements, improvements and other changes to its semiconductor products and this document. This document is confidential and is for the use of the intended customers only. Any disclosure, copying or distribution of this report without HYASIC agreement is strictly prohibited.